

REMARKS

The Office Action of October 15, 2008 was received and carefully reviewed. Claims 1-10, 17-23, 25-27, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50 and 52-64 were pending prior to the instant amendment. By this amendment, claims 3-4 and 21-22 are amended in order to more clearly define the channel length of the first thin film transistor. Support for the aforementioned amendments is found, at least, in Applicant's originally filed specification at paragraph [0057]. Claim 54 is canceled. Consequently, claims 1-10, 17-23, 25-27, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50, 52-53, and 55-64 are currently pending in the instant application, of which, claims 17-23 and 25-27 are withdrawn from consideration. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1, 5, 33 and 44 were rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki et al. (U.S. Patent No. 5,790,213, herein after Sasaki). Sasaki, however, fails to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claims 1, 33, and 44 recites a combination that includes, among other things, an electroluminescence element of the present application which is not taught by Sasaki.

Turning to the Office Action, the Examiner alleges that Sasaki teaches an electroluminescence element in lines 43 to 46 in column 8 of Sasaki. However, this paragraph clearly discloses that the pixel of Sasaki has a liquid crystal and a polarizing plate having a function to polarize the incident light. Thus, one of ordinary skill understands that in a liquid crystal display of Sasaki, incident light is supplied by a backlight fabricated **outside** the pixel, and the backlight is not electrically connected to the second thin film transistor provided in each of the pixels. Furthermore, the operation of the backlight is

independent from the operation of each of the pixel. There is no evidence which shows that the backlight of Sasaki is electrically connected to and operated by the second thin film transistor which is provided in each of the pixels as recited by Applicant's claims.

To establish anticipation under 35 U.S.C. § 102(b), the Examiner must show that each and every feature recited in these claims is either explicitly disclosed or "necessarily present" in a single prior art reference, such as within the four corners of the Sasaki patent. See M.P.E.P. § 2131(7th ed. 1998); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999); *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991). To support a conclusion of anticipation, the Examiner must specifically identify "substantial evidence" setting forth why and how the single prior art reference anticipates each and every feature recited in the claims. See *In re Mullin*, 481 F.2d 1333, 1336-37 (CCPA 1973) (An Examiner's bare assertion that claims were obviously anticipated by a reference did not inform the Applicant as to why the claims lacked novelty); *Dickinson v. Zurko*, 527, U.S. 150 (1999) (The U.S. Patent Office's findings of fact must be reviewed by the substantial evidence standard).

Viewed against this backdrop, each of the Examiner's factual conclusions must be supported by "substantial evidence" in the documentary record. See *In re Lee*, 61 U.S.P.Q.2d 1430, 1432 (Fed. Cir. 2002). The Examiner has the burden of documenting all findings of fact necessary to support a conclusion of anticipation or obviousness "less to 'haze of so-called expertise' acquire insulation from accountability." *Id.* To satisfy this burden, the Examiner must specifically identify where support is found within the prior art to meet the requirements of 35 U.S.C. §§ 102(b). In this case, however, the Examiner cannot satisfy his burden of demonstrating how Sasaki, taken alone or in combination with any other prior art reference, can either render obvious each and every one of the limitations present in the

claims as required by the Manual of Patent Examining Procedure (“MPEP”) and Federal Circuit jurisprudence.

For anticipation under 35 U.S.C. § 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present (M.P.E.P. 706.02). Since each and every element, as set forth in the claims are not found either expressly or inherently described as required by the M.P.E.P., Sasaki cannot be said to anticipate the invention as claimed. Hence, withdrawal of the rejection is respectfully requested.

Claims 2, 3-4, 6-7, 34, 38, 45, 49 and 55-64 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sasaki in view of Luo. However, dependent claims 34, 45, 55, 59, and 62 rely upon one of independent claims 1, 33 and 44 which recite a specific combination of features that distinguishes the invention from Sasaki in different ways as outlined above.

Sasaki in view of Luo, however, fail to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claims 2, 3, 38, and 49 recite a combination that includes, among other things, an electroluminescence element of the present application which is not taught by Sasaki as outlined above. Luo fails to cure the deficiencies of Sasaki by disclosing the missing elements of Sasaki.

Furthermore, as to claim 56, this claim recites that the top surface **in a region between the channel regions** is entirely in contact with the gate insulating film. FIG. 7 of Sasaki fails to show a plurality of channel regions. Hence, Sasaki fails to disclose for fairly suggest the elements as recited in claim 56. Similarly, claims 58 to 60 and their independent claims 33, 38, and 41, respectively, recite at least two gate electrodes, and claims 58 to 60

recite the top surface of the active layer **in a region between the two gate electrodes** to be entirely in contact with the gate insulating film. Since it is apparent that FIG. 7 of Sasaki shows only a single gate electrode 21, Sasaki fails to disclose or fairly suggest the claimed elements of claims 58 to 60.

As to claims 61 to 63, their independent claims 44, 49, and 52, respectively, claim at least two thin film transistors. In claims 61 to 63, these transistors are each limited to have a gate electrode, and these claims further limit the top surface of the active layer **in a region between these gate electrodes** to be entirely in contact with the gate insulating film. In contrast, FIG. 7 of Sasaki shows only a single gate electrode. Hence Sasaki does not disclose the top surface of the active layer in a region between two gate electrodes as claimed. At the very least, the applied references, whether taken alone or in combination, fail to disclose or suggest any of these exemplary features recited in claims.

The Examiner has failed to establish a *prima facie* case of obviousness for at least four reasons. First, the Examiner has not demonstrated how the cited prior art, whether taken alone or in combination, disclose or suggest each and every feature recited in the claims. *See* M.P.E.P. § 2143 (8th ed. 2007). Second, the Examiner has not shown the existence of any reasonable probability of success in modifying the base reference, based on the teachings of the secondary references, in a manner that could somehow result in the claimed invention. *See id.* Third, the Examiner has not identified any suggestion or motivation, either in the teachings of the applied references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the base reference in a manner that could somehow result in the claimed invention. *See id.* Finally, the Examiner has not explained how his obviousness rationale could be found in the prior art — rather than being a hindsight reconstruction of Applicants' own disclosure. *See id.*

Each of the Examiner's factual conclusions must be supported by "substantial evidence" in the documentary record, as required by the Federal Circuit. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2002). The Examiner has the burden of documenting all findings of fact necessary to support a conclusion of anticipation or obviousness "less the 'haze of so-called expertise' acquire insulation from accountability." *Id.* To satisfy this burden, the Examiner must specifically identify where support is found within the prior art to meet the requirements of 35 U.S.C. §§ 102(b) and 103. In this case, however, the Examiner has failed to satisfy his burden of demonstrating how the cited prior art, taken alone or in combination, can either anticipate or render obvious each and every one of the limitations present in present claims, as required by the M.P.E.P. and Federal Circuit jurisprudence.

In accordance with the M.P.E.P. § 2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 409 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 196 (CCPA 1970). Therefore, it is respectfully submitted that none of the cited prior art references, taken alone or in any proper combination, discloses or suggests the subject matter as recited in the claims. Hence, withdrawal of the rejection is respectfully requested.

Claims 1, 5, 33 and 44 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of co-pending Application No. 10/980,603.

Claims 1, 5, 8, 33, 35 and 44 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of co-pending Application No. 10/337,391.

Claims 1-10, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50 and 52-53 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 17-30 of co-pending Application No. 11/258,933.

Claims 2-4, 34, 38-39, 45, 49 and 50 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of co-pending Application No. 10/980,603.

Claims 2-4, 31, 34, 36, 38-39, 42, 45, 47, 49, 50 and 53 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of co-pending Application No. 10/337,391.

Applicant respectfully requests that these rejections be held in abeyance until otherwise allowable claims are designated in the instant application.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore requests the entry of this response, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

In discussing the specification, claims, and drawings in this response, it is to be understood that Applicant in no way intends to limit the scope of the claims to any exemplary embodiments described in the specification and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

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